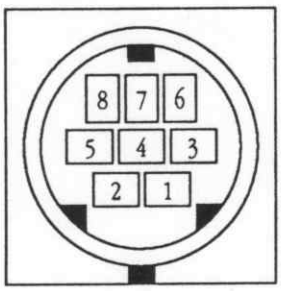
The Macintosh serial interface is controlled by a Zilog Z8530 Serial Communications Controller (SCC) integrated circuit. The SCC provides two serial ports: SCC Port A—the modem port—and SCC Port B—the printer port. Each SCC port has a connector, located on the back panel, for connecting serial peripheral devices and for connecting the computer to the AppleTalk network.

Serial port connectors

All current Macintosh models use miniature 8-pin connectors for their serial ports. Those mini 8-pin connectors provide an output handshake signal not available on the serial ports of the earlier Macintosh computers (Macintosh 128K, 512K, and 512K enhanced); on the other hand, the mini 8-pin connectors do not provide the +5 volts and +12 volts provided by the serial ports of the earlier Macintosh computers.

Figure 10-1 shows the pinout for the mini 8-pin connectors used for the Macintosh serial ports; Table 10-1 shows the signal assignments. These signals are described in the next section, "Signals on the Serial Ports."

■ **Figure 10-1** Pinout for Macintosh mini 8-pin serial port connectors



■ **Table 10-1** Signals on the Macintosh mini 8-pin serial port connectors

Pin number	Signal name	Signal description
1	HSKo	Handshake output. Connected to SCC's RTS; Tri-stated when DTR is inactive; Voh = 3.6V; Vol = –3.6V; Rl = 450Ω
2	HSKi	Handshake input or external clock. Connected to SCC's CTS and TRxC; Vih = 0.2V; Vil = –0.2V; Ri = 12KΩ
3	TxD–	Transmit data (inverted). Connected to SCC's TxD; Tri-stated when DTR is inactive; Voh = 3.6V; Vol = –3.6V; Rl = 450Ω
4	GND	Signal ground. Connected to logic and chassis ground.
5	RxD–	Receive data (inverted); Connected to SCC's RxD; Vih = 0.2V; Vil = –0.2V; Ri = 12KΩ
6	TxD+	Transmit data. Connected to SCC's TxD; Tri-stated when DTR is inactive; Voh = 3.6V; Vol = –3.6V; Rl = 450Ω
7	GPi*	General purpose input.* Connected to SCC's DCD; Vih = 0.2V; Vil = –0.2V; Ri = 12KΩ
8	RxD+	Receive data. Connected to SCC's RxD. Vih = 0.2V; Vil = –0.2V; Ri = 12KΩ

* On the serial port of the Macintosh Plus, pin 7 is not connected.

Signals on the serial ports

The transmit-data and receive-data lines of the Macintosh serial interface conform to the EIA standard RS-422, which differs from the more commonly used RS-232-C standard in that, whereas an RS-232-C transmitter modulates a signal with respect to a common ground, an RS-422 transmitter modulates the signal against an inverted copy of the same signal (to generate a differential signal). The RS-232-C receiver senses whether the received signal is sufficiently negative with respect to ground to be a logical 1, whereas the RS-422 receiver simply senses which line is more negative than the other. An RS-422 signal is therefore more immune to noise and interference, and degrades less over distance, than an RS-232 signal.

The serial data inputs and outputs of the SCC are connected to the external connectors through differential line drivers and receivers. On the Macintosh Plus and Macintosh SE, the drivers are 26LS30 and 9636A ICs and the receivers are 26LS32 ICs; on the Macintosh II, Macintosh IIx, Macintosh IIcx, and Macintosh SE/30, the line drivers are all 26LS30 ICs and the receivers are 75175 ICs. The line drivers can be put in the high-impedance mode between transmissions to allow other AppleTalk devices to transmit over those lines. A line driver is enabled by lowering the SCC's Request To Send (RTS) output for that port.

Inside the SCC chip, port A (the modem port) has a higher interrupt priority than port B, making port A more suitable for high-speed communication. Whenever interrupts are turned off for longer than 100 microseconds, the serial driver stores any data received through port A for later handoff to the port-A input driver. The higher interrupt priority of port A affects only the internal operations of the SCC, and has no effect on the interrupt priority of the SCC in the Macintosh device-interrupt scheme.

On the Macintosh SE, Macintosh II, and more recent models, serial port A supports synchronous transmission, but port B does not; see the discussion of the GPi signal, later in this section. The Macintosh Plus and earlier models do not support synchronous transmission on either port.

Other than the two differences just described, port A and port B are identical.

The Output Handshake signal (HSKo) for each Macintosh Plus serial port originates at the SCC's Data Terminal Ready (DTR) output for that port and is driven by an RS-422 line driver. On the Macintosh Plus and the Macintosh SE, it's a 3488A or 9636A; on the Macintosh SE/30, Macintosh II, Macintosh IIx, and Macintosh IIcx it's a differential line driver (26LS30).

Each port's Input Handshake signal (HSKi) is connected to the SCC's Clear To Send (CTS) input for that port, and is designed to accept an external device's Data Terminal Ready (DTR) handshake signal. This line is also connected to the SCC's Transmit/Receive Clock (TRxC) input for that port, so that an external device can perform high-speed synchronous data exchange. Note that you can't use the HSKi line for receiving DTR if you're using it to receive a high-speed data clock.

Except on the Macintosh Plus and earlier models, each serial port also has a general-purpose input (GPi, pin 7), connected to the SCC's Data Carrier Detect (DCD) input for that port. This input can be used to provide a handshake signal from an external device to the computer. The DCD input to the SCC can be polled by software or can be used to generate a CPU interrupt.

- *Note:* On the Macintosh Plus and earlier Macintosh computers, the GPi signal is not connected. On those computers, the DCD inputs to the SCC are used to generate mouse interrupts, as described in the section "Macintosh Plus Mouse" in Chapter 7. In the other Macintosh models, each DCD input to the SCC is brought out to a pin on a serial port connector.

On port A only, the GPi line can be connected to the SCC's Receive/Transmit Clock (RTxCA). This feature supports devices, such as synchronous modems, that provide separate transmit and receive data clocks. Bit 3 (vSync) of VIA Data register A, when set low, connects GPiA to RTxCA. When the VIA vSync bit is set high, RTxCA is connected to a 3.672 MHz clock. Port B's Receive/Transmit clock (RTxCB) is always connected to the 3.672 MHz clock, as in the classic Macintosh configuration. Note that you can't use the Gpi line to receive a DCD input when you are using it to receive a high-speed clock. This input is noninverting for compatibility with the classic Macintosh configuration. The general purpose input (GPi) is received by means of the negative (inverting) input of one of the same differential receivers, with the positive input grounded.

△ Tip Because the 26LS32 is a differential receiver, any handshake or clock signal driving it must be bipolar, alternating between a positive voltage and a negative voltage with respect to the internally grounded input. If a device uses ground (0 volts) as one of its handshake logic levels, the receiver interprets that level as an indeterminate state, with unpredictable results. △

The SCC chip generates level-2 processor interrupts (/IPL1) during I/O over the serial lines. During disk accesses, the disk controller disables all interrupts of level 3 and lower to prevent any loss of data that might occur when the CPU pauses to service an interrupt. Because the SCC chip cannot store more than 3 bytes of incoming data, however, and because serial data (such as an AppleTalk message) might come in at any time, it may be necessary to service the SCC before a floppy disk transaction is complete. To allow software to determine whether there is a byte of serial data waiting to be read, therefore, the VIA monitors the SCC's Wait/Request line. Whenever there is a pause in a floppy disk transaction, the disk driver can check bit 7 in VIA Data register A to determine the state of the Wait/Request line. If there is data waiting in the SCC, the driver reads it during the next pause in the disk transaction.

The maximum nominal data transmission rate that you can select through the Macintosh Toolbox is 57,600 baud. This is the maximum rate that the classic Macintosh computers can maintain for transmission of serial data when the SCC port is operating in an asynchronous, interrupt-driven fashion, timed by the 3.672 MHz clock.

AppleTalk operates at a nominal data transmission rate of 230.4 Kbaud. This higher rate is possible because AppleTalk communications are not interrupt driven; during AppleTalk communications, the AppleTalk Driver has complete control of the computer. Although AppleTalk uses a synchronous communication protocol, the AppleTalk Driver runs the SCC chip in asynchronous mode, timed by the 3.672 MHz clock.

The maximum possible transmission rate for serial data ranges from approximately 500 Kbaud on the Macintosh Plus and Macintosh SE to 900 Kbaud on the Macintosh II. To achieve such data transmission rates, the SCC would have to be operated in synchronous mode timed by an external clock, and the serial driver would have to have complete, uninterrupted control of the computer.

SCC Addresses

This section describes the way low-level programs—serial drivers—control the serial interface. It is provided for the sake of completeness only. Unless you are writing your own driver software, you should never need to use the information is this section. For more information about the SCC chip, see the product specification for the Zilog Z8530 Serial Communications Controller.

△ Tip Unless you need to write your own driver software, it is much easier and safer to use the driver routines and ROM tools provided by the Macintosh Operating System to access the hardware devices in the Macintosh. If you do need to write drivers, you should communicate directly with Apple to obtain technical assistance. See the section, "Apple Developer Services," at the end of the Preface. △

The addresses of the SCC control and data registers are given in Table 10-2 as offsets from the constant sccWBase for writes, or sccRBase for reads. These base addresses are also available in the global variables SCCWr and SCCRd.

■ **Table 10-2** Addresses of SCC registers

Location	Register
sccWBase+aData	Write Data register A
sccRBase+aData	Read Data register A
sccWBase+bData	Write Data register B
sccRBase+bData	Read Data register B
sccWBase+aCtl	Write Control register A
sccRBase+aCtl	Read Control register A
sccWBase+bCtl	Write Control register B
sccRBase+bCtl	Read Control register B

Note: On the Macintosh models with MC68000 microprocessors, using the address offsets shown in this table automatically supplies the correct even or odd address for each access.

△ Tip On the Macintosh Plus and earlier Macintosh models, it is necessary to let the SCC lines stabilize for 2.2 µs between accesses. On later models, it is not necessary to do so because the general logic IC (GLU or BBU) delays the acknowledge signal (/DTACK or /DSACK0) until the SCC lines have stabilized. △

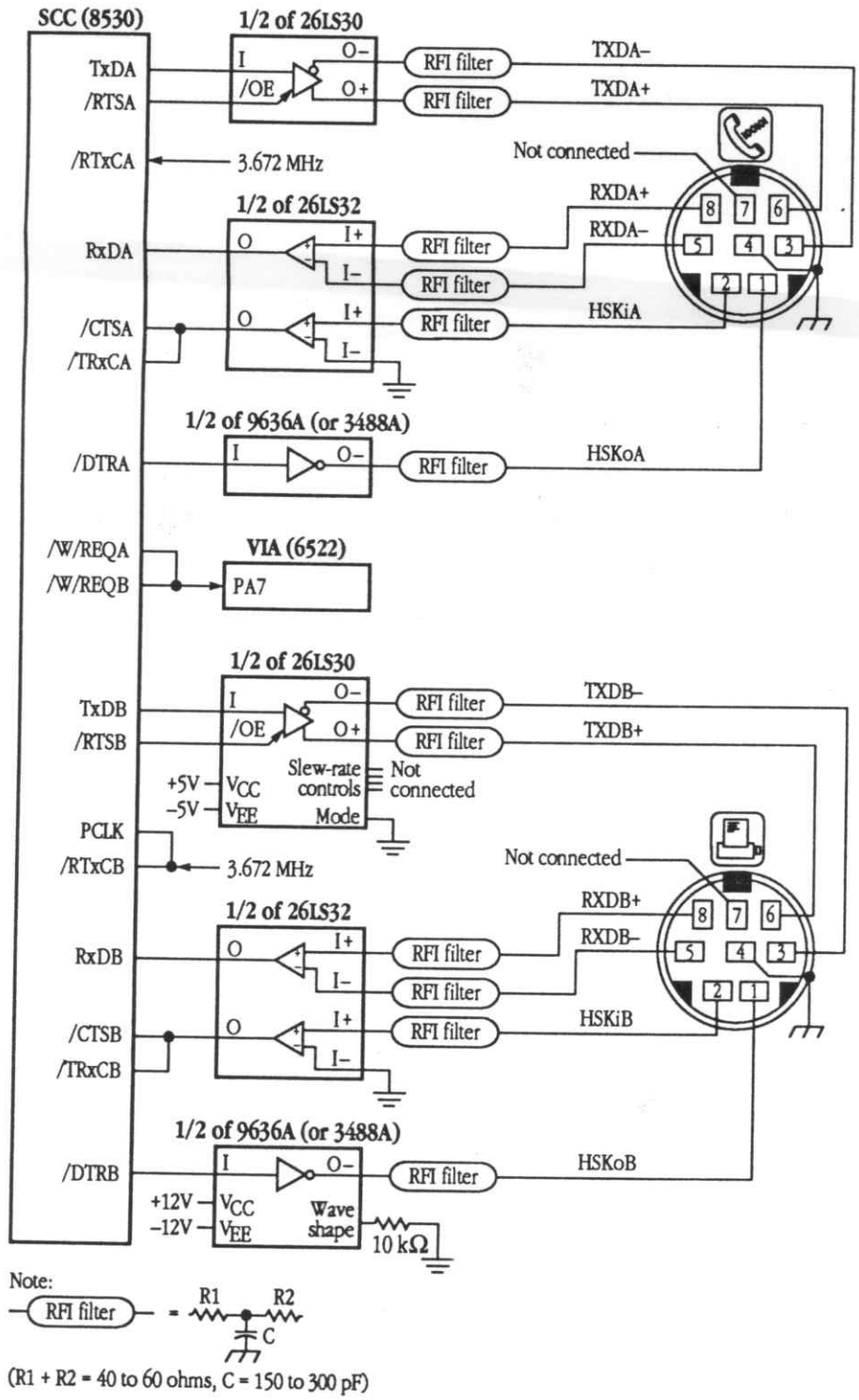
On Macintosh models with MC68000 microprocessors, you must use even-addressed byte-wide accesses to read data from the SCC and odd-addressed byte-wide accesses to write data to the SCC. Although the SCC is on only the upper byte of the data bus, this scheme works because the MC68000 CPU reads from the upper byte of the data bus when reading from an even address, and puts the same data on both bytes of the data bus when writing to an odd address. A byte-wide read from an odd address resets the SCC.

△ Tip In Macintosh models with MC68000 microprocessors, be careful never to make a word-wide access to the SCC. A word-wide access to any SCC address causes a phase shift in the processor clock in those models (a feature used by the operating system during system startup to ensure correct RAM-access timing). An incorrect phase shift causes an unstable video display, RAM errors, and VIA errors. △

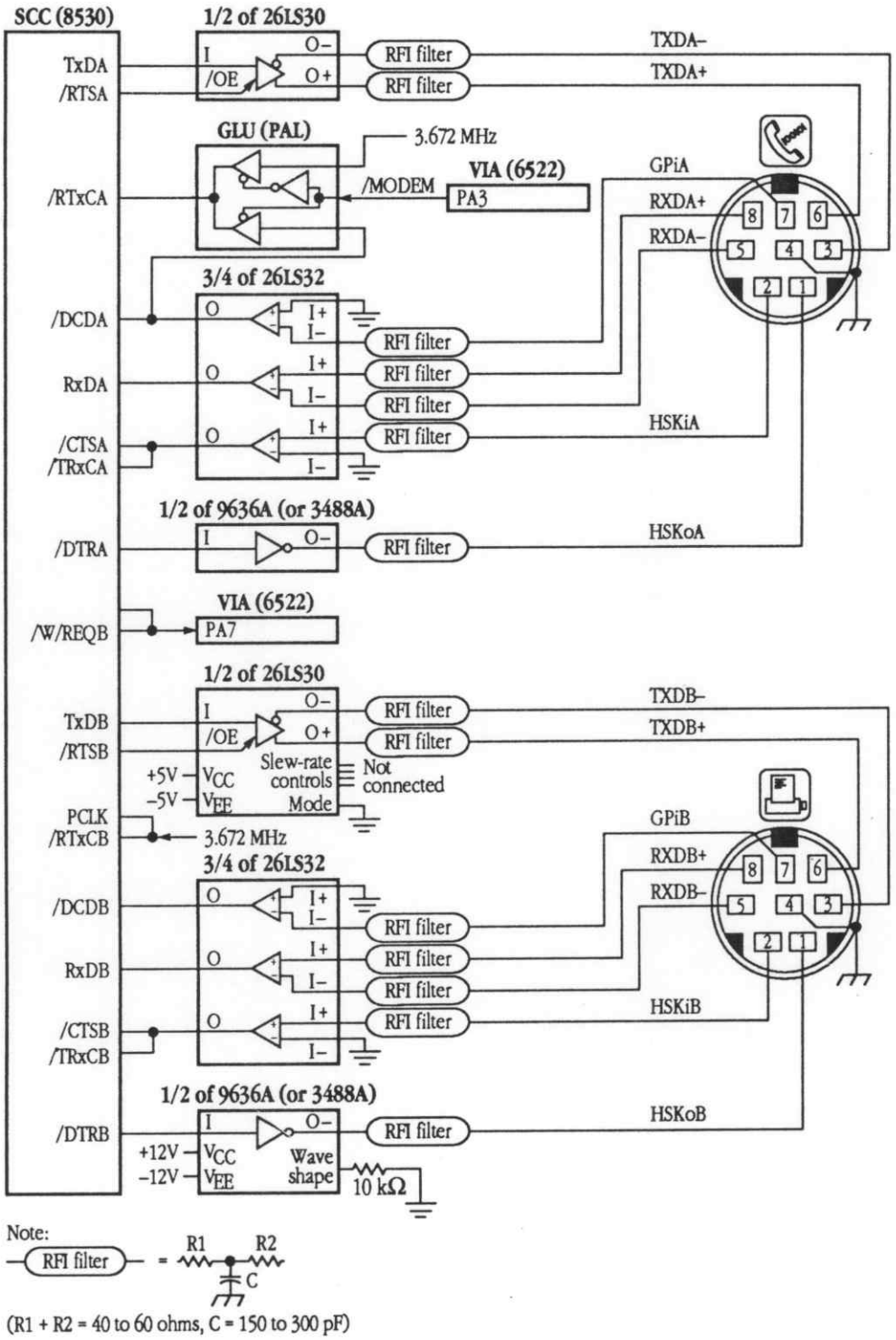
Serial port circuit diagrams

Figure 10-2 shows a circuit diagram of the serial interface used in the Macintosh Plus. Figure 10-3 shows a circuit diagram of the serial interface used in the Macintosh SE. Figure 10-4 shows a circuit diagram of the serial interface used in the Macintosh II, Macintosh IIx, Macintosh IIcx, and Macintosh SE/30 computers.

■ **Figure 10-2** Circuit diagram of the serial interface in the Macintosh Plus computer



■ **Figure 10-3** Circuit diagram of the serial interface in the Macintosh SE computer



■ **Figure 10-4** Circuit diagram of the serial interface in the Macintosh II, Macintosh IIx, Macintosh IIcx, and Macintosh SE/30 computers